Si9121 Demonstration Board

FEATURES

- –10-V to –60-V Input Voltage Range
- Fixed +5-V or +3.3-V Output
- Output load up to 400 mA
- Current Mode Control
- On-Chip 70-V, 1.5-Ω N-Channel MOSFET Switch
- High Efficiency Operation
- Integrated Floating Feedback Amplifier
- Integrated High Voltage Start-Up Circuit, with V_{CC} Regulator
- 95-kHz fixed frequency PWM Operation
- Under Voltage Lockout
- Hiccup Mode Short Circuit Protection
- Thermal Shutdown
- SOIC-8 Narrow-Body Package

DESCRIPTION

The Si9121DY is a non-isolated buck-boost converter IC, operating from a wide input voltage range of –10 to –60 V with minimal external components. This polarity inverter converts –48 V to +5 V or +3.3 V, making it suitable for applications including digital phones and ISDN power supplies. A non-isolated buck-boost design with the Si9121 eliminates the need for an expensive transformer, while its integrated low on-resistance MOSFET driver, floating feedback error amplifier, fixed-frequency oscillator, output voltage sensing resistor divider, and depletion mode MOSFET for start up/V_{CC} regulation reduce the external component count to less than 10. The V_{CC} can be generated using a coupled inductor, with additional winding. This will reduce the power dissipation in the internal V_{CC} regulator and improve the efficiency, especially at a lower load current. Other applications include the flyback converter.

The demonstration boards use surface mount and through hole components and is fully assembled and tested for quick evaluation. The test points are provided for the closed loop response measurement.

Included in this document are the Bill-Of-Material, Schematics, PCB Layout of the demo boards and some of the actual waveforms.

The demonstration board layout is available in Gerber file format. Please contact your Vishay Siliconix sales representative or distributor for a copy.

ORDERING INFORMATION: **Si9121DB-5** (V_{OUT} = 5 V/400 mA)
Si9121DB-3 (V_{OUT} = 3.3 V/400 mA)

POWER-UP CHECK LIST

The Si9121DB-5 and Si9121DB-3 are both designed to operate in continuous mode at high line and full load condition. Follow the same procedure as described for both the demo board operation.

1. Visually inspect the PCB to be sure that all the components are intact and no foreign substance is lying on the board.
2. Solder the leads at U1-pin 8/inductor L1 to monitor the MOSFET drain waveform on the oscilloscope.
3. Reduce the source voltage to zero and connect the positive through the dc ammeter at GND (P1) and negative to $–V_{IN(P2)}$. Connect the dc voltmeter at exactly across P1 and P2.
4. Connect the voltmeter exactly across $+V_{OUT(P-4)}$ and GND(P3) for the output voltage measurement. Connect the load through dc ammeter across P4 and P3, with positive at $+V_{OUT(P4)}$. Increase the load current to 200 mA.

5. Connect the oscilloscope ground to $-V_{IN(P2)}$, while the probe to U1-pin8/ inductor L1 to observe the switching waveform.
6. Slowly increase the input voltage while monitoring the input current meter and continue to increase the voltage further till the circuit turns an at around 9.5 V.
7. Set the input voltage to 48-V nominal and monitor the drain waveform, switching frequency.
8. When observing the output Ripple/Noise, remember to remove the oscilloscope ground from $-V_{IN(P2)}$.
9. The efficiency, line and load regulation can be measured by varying the line between 10 to 60 V, and the load between 0 to 400 mA.

TYPICAL WAVEFORMS AND PERFORMANCE

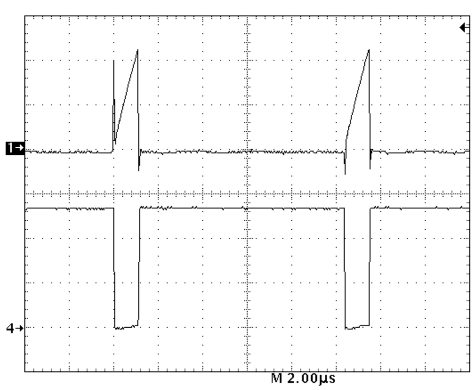
Drain Voltage and Current

The circuit is designed to operate in the continuous mode at all line and full load. Refer to Figure 1 for the drain voltage and current waveforms at 48 V_{IN} and 400-mA load. The current step at MOSFET turn on indicates the continuous mode operation.

Output Regulation

The output load regulation is tight, since it is sensed right at the $+V_{OUT}$. Figures 2 and 3 depicts line and load regulation. The load regulation is within specification even at zero load since the IC draws some current from the V_{OUT} (Pin5).

The output voltages are essentially constant with respect to any variation of input voltage and output load in case of both demo boards.



V_{IN} = 48 V
V_{OUT} = 5 V/400 mA
Ch 1 = MOSFET Current (0.4 A/div)
Ch 4 = Drain Voltage (20 V/div)

Figure 1. Drain Voltage and Current

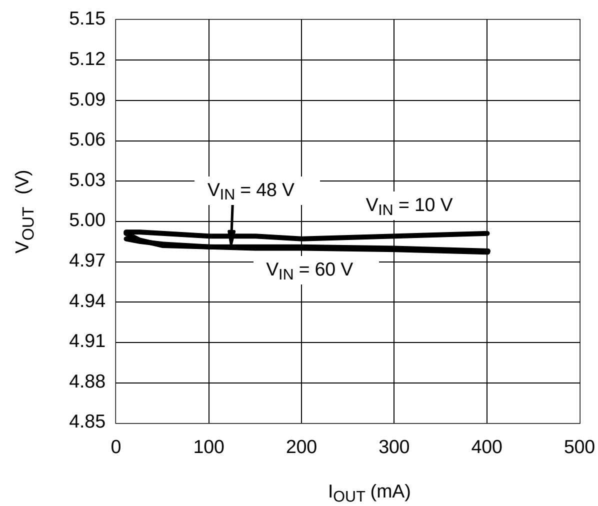


Figure 2. V_{OUT} (5 V) Line/Load Regulation—Si9121DB–5

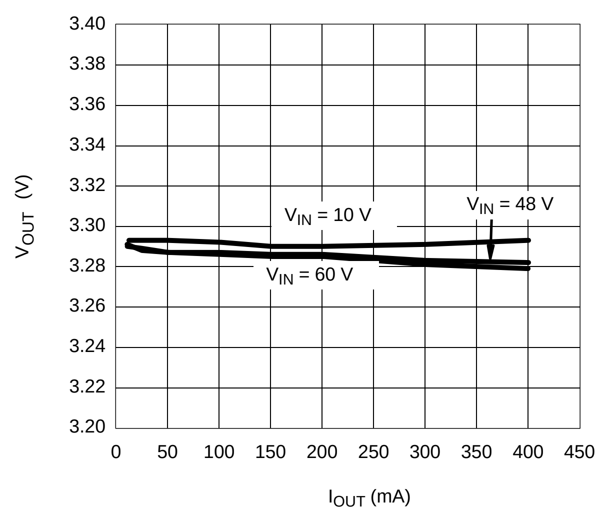
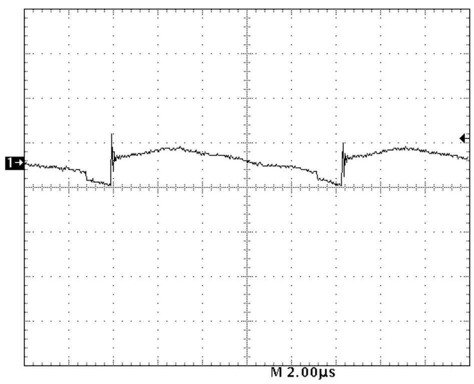


Figure 3. V_{OUT} (3.3 V) Line/Load Regulation—Si9121DB–5

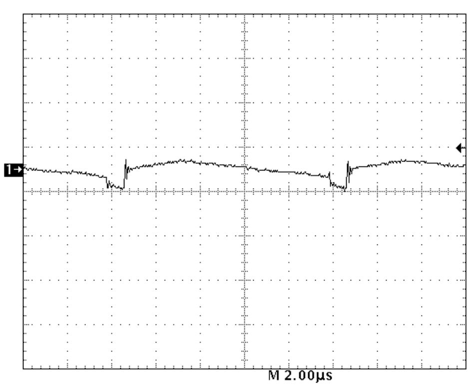
Output Ripple and Noise

The tantalum chip capacitors are used for lower ESR and higher ripple current capability. Lower cost of aluminium capacitors can also be used where form factor and/or output ripple are of secondary importance. Also, a small additional LC filter can be added at 5-V or 3.3-V output for further attenuation ac component by even 5 to 10 times. The Si9121DB-5 (Figure 4) and Si9121DB-3 (Figure 5) show the ripple at a full load and 48-V input.



V_{IN} = 48 V
V_{OUT} = 5 V/400 mA
Ch 1 = 50 mV/div

Figure 4. Output Ripple and Noise—Si9121DB–5



V_{IN} = 48 V
V_{OUT} = 3.3 V/400 mA
Ch 1 = 50 mV/div

Figure 5. Output Ripple and Noise—Si9121DB–3

Efficiency

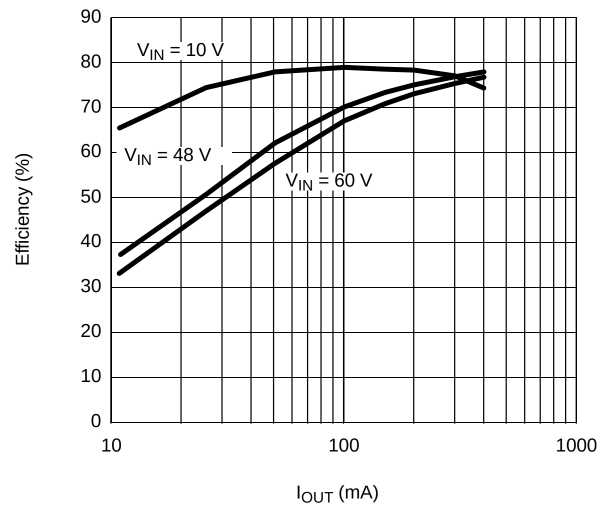


Figure 6. Converter Output Load vs Efficiency—Si9121DB–5

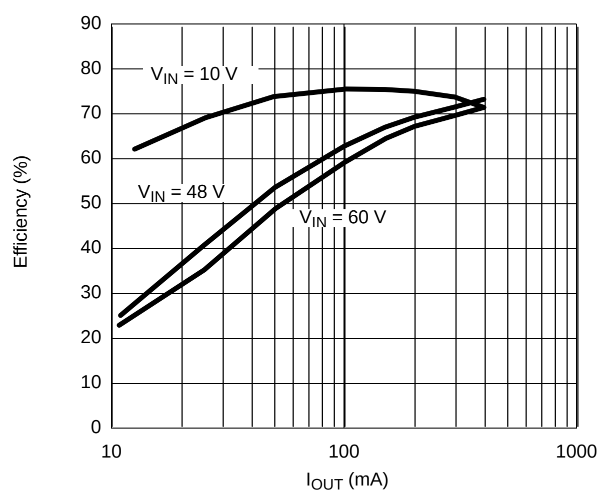


Figure 7. Converter Output Load vs Efficiency—Si9121DB–3

The Efficiency of the converter, can be improved further by adding the V_{CC} winding to the inductor. The external V_{CC} at pin 7 and $-V_{IN}$, reduces the power loss by switching off the internal V_{CC} regulator. The Figure 8 depicts the efficiency improvement.

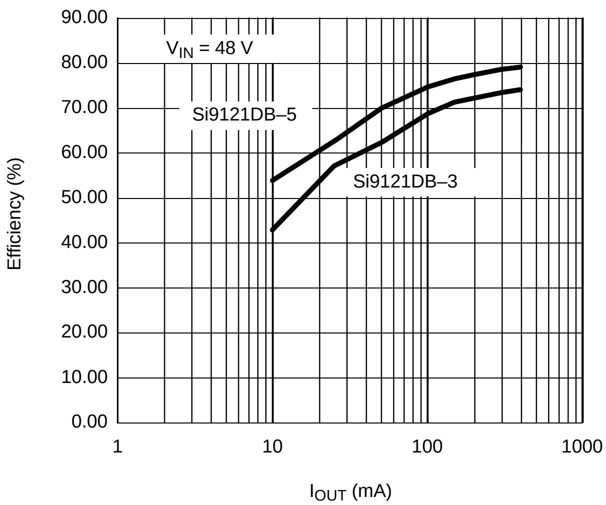
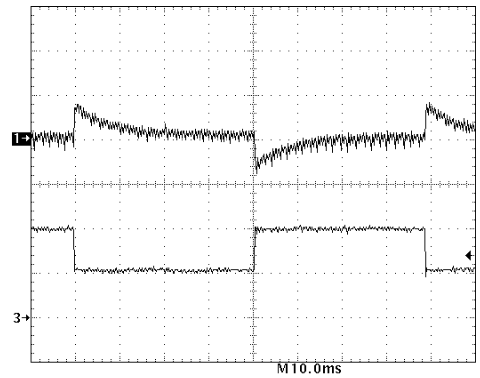
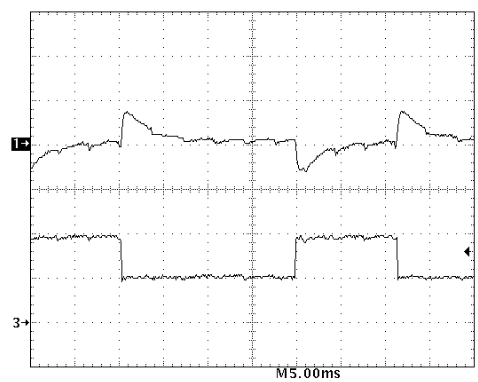


Figure 8. Efficiency Using External Vcc—Si9121DB–5 and Si9121DB–3



V_{IN} = 48 V
V_{OUT} = 5 V
Step Load = 200 to 400 mA
Ch 1 = V_{OUT} (100 mV/div)
Ch 3 = V_{OUT} (200 mV/div)

Figure 9. Dynamic Load Response—Si9121DB–5



V_{IN} = 48 V
V_{OUT} = 3.3 V
Step Load = 200 to 400 mA
Ch 1 = V_{OUT} (200 mV/div)
Ch 3 = V_{OUT} (200 mV/div)

Figure 10. Dynamic Load Response—Si9121DB–3

Dynamic Load Response

The converter output is monitored while applying the step load of 200 to 400 mA. The current step and output voltage deviation is captured on the oscilloscope with 100-MHz bandwidth.

SCHEMATIC

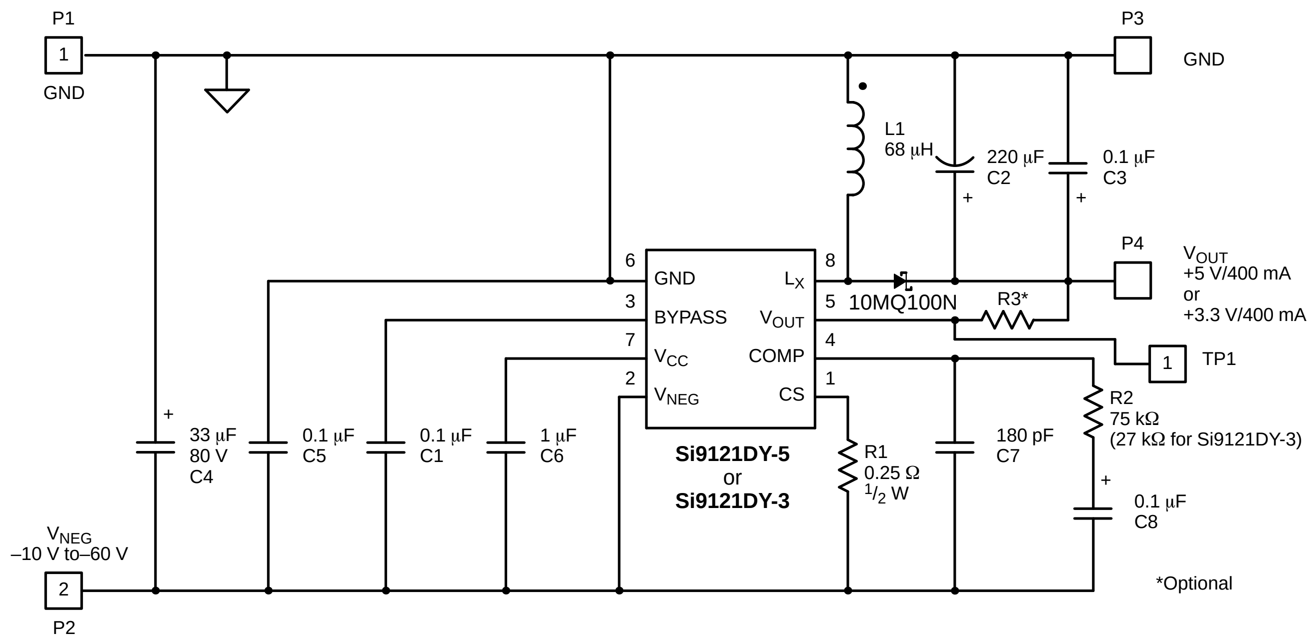


Figure 11. Typical Applications Circuit—Si9121DB

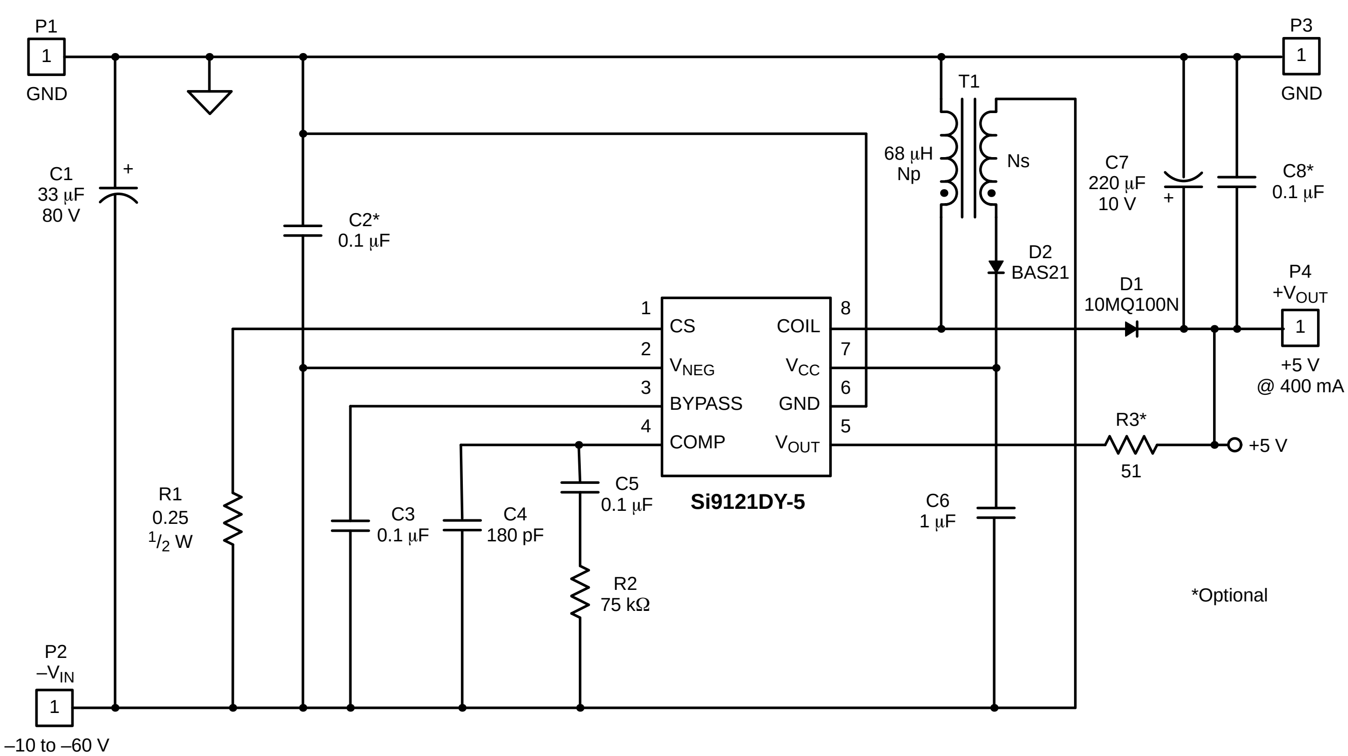


Figure 12. Schematic Si9121DB-5 and Si9121DB-3 with External Vcc

TABLE 1. BILL-OF-MATERIALS

Item	Qty	Designator	Part Type	Description	Footprint	Vendor Part#	Manufacturer
1	1	R1	0.25 Ω	RES,1%, 1/2W, PWER Metal Strip	WSL-2010	WSL-2010	Vishay Dale
2	1	R2	75 kΩ	RES,1%, 1/8 W	0805	CRW08057502RF	Vishay Dale
			27 kΩ for Si9121-3	RES,1%, 1/8 W	0805	CRW08052702RF	Vishay Dale
3	1	R3	51 Ω	RES,1%, 1/8 W	0805	CRW0805751R0F	Vishay Dale
4	1	C1	33 μF	CAP, ELEC, 80 V, PF	RB.14/.32	UPF1K330MPH6	Nichicon
5	4	C2, C3, C5, C8	0.1 μF	CAP, CER	0805	VJ0805Y104KXXA	Vishay Vitramon
6	1	C4	180 pF	CAP, CER	0805	VJ0805Y181KXXA	Vishay Vitramon
7	1	C6	1 μF	CAP, CER, 50 V	0805	VJ0805Y105KXAAT	Vishay Vitramon
8	1	C7	220 μF	CAP, TAN, 10 V	594D_D	594D227X0010D2T	Vishay Sprague
9	1	D1	10MQ100N	Schottky Diode, 35 V	SMA	10MQ100N	I. R.
10	1	L1	68 μH	Inductor,	IDC5020	IDC5020-68uH	Vishay Dale
11	1	U1	Si9121DY-5 (or Si9121-3)	Power IC	SO-8	SI9121DY-5	Vishay Siliconix

PCB LAYOUT

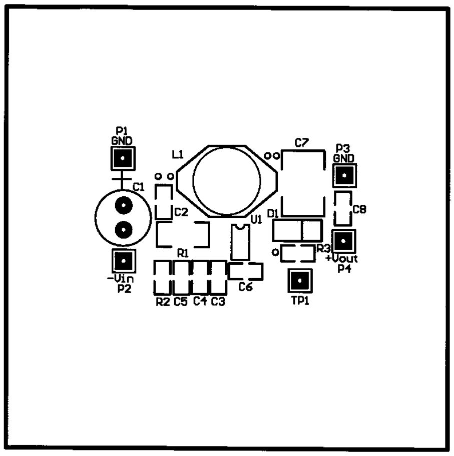


Figure13 Silk Screen—Si9121DB

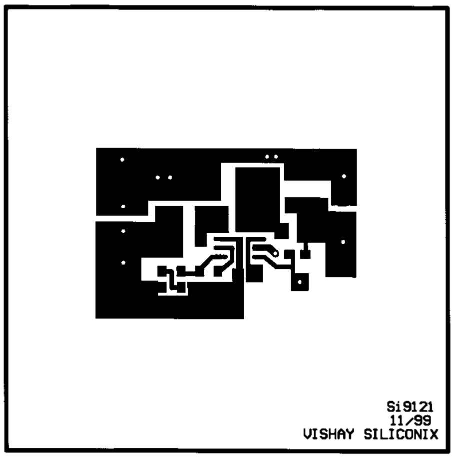


Figure14 Top Layer—Si9121DB

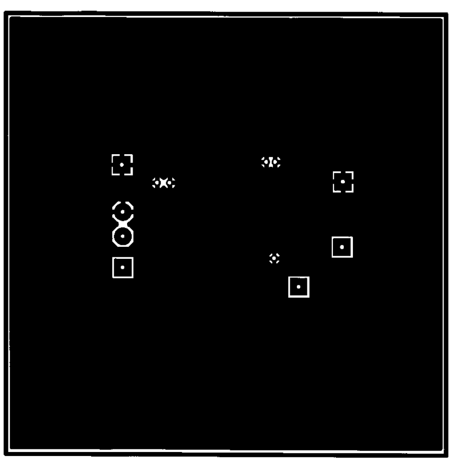


Figure15 Bottom Layer—Si9121DB

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